IN THE CLAIMS

Please cancel Claim 1 without prejudice.

Please add Claims 2-9 as follows:

2. An address pattern generator for a digital data processing system memory having memory elements addressable by column and row locations, said generator including:

a column address generator including:

(a) an initial value register for storing an indication of a lowest column location in which data are stored;

(b) a maximum value register for storing an indication of a highest column location in which data are stored;

(c) an address register for storing a column address location;

(d) a first add circuit connected to said address register for receiving said stored column address therefrom, said first add circuit producing a first incremented column address from said stored column address;

(e) a second add circuit connected to said first add circuit for receiving said first incremented column address therefrom and to said initial value register for receiving said indication of said lowest column location, said second add circuit producing a second incremented column address from said first incremented column address and said lowest column location;

(f) a comparator connected to said first add circuit for receiving said first incremented column address and to said maximum value register for receiving said value representative of said highest column location, said comparator being configured to assert a first comparison signal when said first incremented column address is greater than the highest column location; and

(g) a selector connected to said first add circuit for receiving said first incremented column address therefrom, to said second add circuit for receiving said second incremented column address therefrom, to said column address generator comparator for receiving said first comparison signal therefrom and to said address register for forwarding one of said

incremented column addresses thereto, said selector forwarding either said first or second incremented column address to said address register depending on the state of said first comparison signal; and

a row address generator including:

(a) an initial value register for storing an indication of a lowest row location in which data are stored;

(b) a maximum value register for storing an indication of a highest row location in which data are stored;

(c) an address register for storing a row address location;

(d) a first add circuit connected to said row address generator address register for receiving said stored row address therefrom, said first add circuit producing a first incremented row address from said stored row address;

(e) a second add circuit connected to said row address generator first add circuit for receiving said first incremented row address therefrom and to said initial value register for receiving said indication of said lowest row location, said second add circuit producing a second incremented row address from said first incremented row address and said lowest row location;

(f) a comparator connected to said row address generator first add circuit for receiving said first incremented row address and to said row address generator maximum value register for receiving said value representative of said highest row location, said comparator being configured to assert a second comparison signal when said first incremented row address is greater than the highest row location; and

(g) a selector connected to said row address generator first add circuit for receiving said first incremented row address therefrom, to said row address generator second add circuit for receiving said second incremented row address therefrom, to said row address generator comparator for receiving said ~~first~~ second comparison signal therefrom and to said address register for forwarding one of said incremented row addresses

thereto, said selector forwarding either said first or second incremented row address to said row address generator address register depending on the state of said second comparison signal.

23. The address pattern generator of Claim 1, wherein said row address generator first add circuit includes an adder configured to receive a carry-in addend and said first comparison signal from said column address generator comparator is applied to said row address generator first add circuit to function as said carry-in addend.

24. The address pattern generator of Claim 12 wherein:

said column address generator selector forwards said first incremented column address to said column address generator address register when said first comparator signal is not asserted and forwards said second incremented column address to said column address generator address register when said first comparator signal is asserted; and

said row address generator selector forwards said first incremented row address to said row address generator address register when said second comparator signal is not asserted and forwards said second incremented row address to said row address generator address register when said second comparator signal is asserted.

25. The address pattern generator of Claim 24, wherein:

said column address generator first add circuit includes an operation register and an adder, said operation register storing a column increment value, and said adder is connected to receive said column address from said address register and said column increment value from said operation register as addends and produces said first incremented column address therefrom; and

said row address generator first add circuit includes an operation register and an adder, said operation register storing a row increment value, and said adder is connected to receive said row address from said address register and said row

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increment value from said operation register as addends and produces said first incremented row address therefrom.

16. The address pattern generator of Claim 13, wherein:

said column address generator second add circuit includes a subtracter and an adder, said subtracter being connected to receive said first incremented column address from said first add circuit and to receive said highest column location from said maximum value register so as to produce an intermediate value representative of the difference between said first incremented column address and said highest column location and said adder is configured to receive said intermediate value from said subtracter and said lowest column location from said initial value register as addends and produces said second incremented column address therefrom; and

said row address generator second add circuit includes a subtracter and an adder, said subtracter being connected to receive said first incremented row address from said first add circuit and to receive said highest row location from said maximum value register so as to produce an intermediate value representative of the difference between said first incremented row address and said highest row location and said adder is configured to receive said intermediate value from said subtracter and said lowest row location from said initial value register as addends and produces said second incremented row address therefrom.

17. The address pattern generator of Claim 16, wherein:

said column address generator second add circuit includes a subtracter and an adder, said subtracter being connected to receive said first incremented column address from said first add circuit and to receive said highest column location from said maximum value register so as to produce an intermediate value representative of the difference between said first incremented column address and said highest column location and said adder is configured to receive said intermediate value from said

subtracter and said lowest column location from said initial value register as addends and produces said second incremented column address therefrom; and

said row address generator second add circuit includes a subtracter and an adder, said subtracter being connected to receive said first incremented row address from said first add circuit and to receive said highest row location from said maximum value register so as to produce an intermediate value representative of the difference between said first incremented row address and said highest row location and said adder is configured to receive said intermediate value from said subtracter and said lowest row location from said initial value register as addends and produces said second incremented row address therefrom.

8. The address pattern generator of Claim 7, wherein said row address generator first add circuit includes an adder configured to receive a carry-in addend and said first comparison signal from said column address generator is applied to said row address generator first add circuit to function as said carry-in addend.

9. The address pattern generator of Claim 8, wherein said row address generator first add circuit adder is configured to receive a carry-in addend and said first comparison signal from said column address ~~signal~~ generator is applied to said row address generator first add circuit to function as said carry-in addend.

REMARKS

This paper is filed in response to the Office Action for the above-identified application mailed November 3, 1994.

By way of that Action, the sole claim initially presented for review, Claim 1, was rejected under 35 USC §103 as being unpatentable over U.S. Patent No. 4 300 234 to Maruyama et al. in view of U.S. Patent No. 3 751 649 to Hart, Jr.